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10/606,715	06/26/2003	Benjamin Thomas Percer	200312936-1	5780

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EXAMINER	
LE, JOHN H	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/606,715	PERCER ET AL.	
	Examiner	Art Unit	
	John H. Le	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/28/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. This office action is in response to applicant's amendment received on 02/15/2005.

Claims 1-2, 4-5, 7-12, 14-15, 18, and 20-24 have been amended.

Claims 25-32 have been added.

The Title has been amended.

The specification has been amended.

Claim Objections

2. Claim 28 is objected to because of the following informalities:

Claim 28, line 1, after "The margin testing system of claim 27" should change to – The method of claim 27--.

Appropriate correction is required.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1-32 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 55-75 of U.S. 2004/0267482 A1.

Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 1-32 of prior art anticipate claims 55-75 of instant application as follows:

Instant Application	US 2004/0267482 A1
	55. In an electronic system, a system for margin testing one or more components of the computer system, comprising: a fault bypass module incorporated in said electronic system, said fault bypass module masking signals indicative of faults associated with one or more of said components during margin testing of said electronic system.
1. A margin testing system for margin testing one or more components of an electronic system, comprising: a fault bypass module incorporated in said electronic system, said fault bypass module configured to intercept and mask signals indicative of one or more faults associated with one or more of said components during margin testing of said electronic system.	63. The margin testing system of claim 55, further comprising: a power control element in communication with said fault bypass module, said fault bypass module transmitting one of more of said fault signals to said power control element in absence of margin testing and masking said one or more fault signals during margin testing of said electronic system. 64. The margin testing system of claim 63, wherein said fault bypass module masks said fault signal by intercepting said fault signal and supplying to said power control element a signal indicative of absence of a fault indicated by said fault signal.
2. The margin testing system of claim 1, wherein sate at least one of said one or more faults corresponds to an operating parameter associated with at least one of said one or more components crossing a selected threshold.	56. The margin testing system of claim 55, wherein said at least one of said faults corresponds to an operating parameter associated with at least one of said components crossing a selected threshold.
3. The margin testing system of claim 2, wherein said operating parameter is any of frequency, voltage or temperature.	57. The margin testing system of claim 56, wherein said operating parameter is any of frequency, voltage or temperature.
4. The margin testing system of claim 1, further comprising: a controller incorporated in said electronic system and in communication with said fault bypass module, said controller configured to transmit a command to said fault bypass module to initiate masking of said fault signals by said module.	58. The margin testing system of claim 55, further comprising: a controller internal to said electronic system and in communication with said fault bypass module, said controller transmitting a command to said fault bypass module for initiating masking of said fault signals by said module.
5. The margin testing system of claim 1, wherein said fault signals comprise: one or more interrupt signals.	59. The margin testing system of claim 55, wherein said fault signals comprise: interrupt signals.
6. The margin testing system of claim 1, wherein said fault bypass module permits normal processing of said fault signals during normal operation of said electronic system.	60. The margin testing system of claim 55, wherein said fault bypass module permits normal processing of said fault signals during normal operation of said electronic system.
7. The margin testing system of claim 4, further comprising: a hardware monitor configured to communicate with said controller and with at least one of said one or more components, and to generate a fault on fault signal in response to an occurrence of a fault associated with said at least one component.	61. The margin testing system of claim 58, further comprising: a hardware monitor in communication with said controller and with at least one of said components, said hardware generating an fault signal in response to occurrence of a fault associated with said at least one component.
8. The margin testing system of claim 7, wherein said hardware monitor is further configured to transmit said fault signal to said fault bypass module, and wherein said fault bypass module is further configured to mask said received fault signal during margin testing of said electronic device.	62. The margin testing system of claim 61, wherein said hardware monitor transmits said fault signal to said fault bypass module, said fault bypass module masking said received fault signal during margin testing of said electronic device.
9. The margin testing system of claim 1, further comprising: a power control element configured to communicate with said fault bypass module, and wherein said fault bypass module is further configured to transmit one or of more of said fault signals to said power control element in absence of margin testing and to mask said one or more fault signals during margin testing of said electronic system.	63. The margin testing system of claim 55, further comprising: a power control element in communication with said fault bypass module, said fault bypass module transmitting one of more of said fault signals to said power control element in absence of margin testing and masking said one or more fault signals during margin testing of said electronic system.

10. The margin testing system of claim 9, wherein said fault bypass module is further configured to mask said fault signal by intercepting said fault signal and supplying to said power control element a signal indicative of an absence of a fault indicated by said fault signal.	64. The margin testing system of claim 63, wherein said fault bypass module masks said fault signal by intercepting said fault signal and supplying to said power control element a signal indicative of absence of a fault indicated by said fault signal.
11. The margin testing system of claim 7, wherein said at least one component is a power rail, and said hardware monitor is further configured to generate an interrupt signal in response to a voltage associated with said power rail varying from a nominal value by more than a selected threshold.	65. The margin testing system of claim 61, wherein said at least one component is a power rail, and said hardware monitor generates an interrupt signal in response to a voltage associated with said power rail varying from a nominal value by more than a selected threshold.
12. The margin testing system of claim 11, wherein said power control module is further configured to reduce power applied to said power rail in response to said interrupt signal in the absence of margin testing.	66. The margin testing system of claim 65, wherein said power control module lowers power applied to said voltage rail in response to said interrupt signal in the absence of margin testing.
13. The margin testing system of claim 1, wherein said fault bypass module comprises: a programmable logic device programmed to provide masking of said fault signals.	67. The margin testing system of claim 55, wherein said fault bypass module comprises: a programmable logic device programmed to provide masking of said fault signals.
14. The margin testing system of claim 7, further comprising a temperature diode coupled to at least one of said components and configured to measure a temperature of said component and to supply said measured temperature to said hardware monitor.	68. The margin testing system of claim 61, further comprising a temperature diode coupled to at least one of said components and said hardware monitor for measuring a temperature of said component and supplying said measured temperature to said hardware monitor.
15. (Currently Amended) The margin testing system of claim 7, wherein said fault bypass module is further configured to intercept a selected output signal of said at least one component and to generate a simulated signal corresponding to said intercepted output signal for transmittal to said hardware monitor during margin testing of said component.	69. The margin testing system of claim 61, wherein said fault bypass module intercepts a selected output signal of said at least one component and generates a simulated signal corresponding to said intercepted output signal for transmittal to said hardware monitor during margin testing of said component.
16. The margin testing system of claim 1, wherein said electronic system comprises a computer system.	70. The margin testing system of claim 55, wherein said electronic system comprises a computer system.
1 7. The margin testing system of claim 15, wherein said computer system is a computer server.	71. The margin testing system of claim 69, wherein said computer system is a computer server.
18. The margin testing system of claim 4, wherein said controller comprises: a Baseboard Management Controller (BMC).	72. The margin testing system of claim 58, wherein said controller comprises: a BMC
19. The margin testing system of claim 18, further comprising: a communication bus for providing communication between said BMC and said fault bypass module.	73. The margin testing system of claim 72, further comprising: a communication bus for providing communication between said BMC and said fault bypass module.
20. The margin testing system of claim 19, wherein said communication bus is ~ an Inter-Integrated Circuit (I^2C)-based bus.	74. The margin testing system of claim 73, wherein said communication bus is an I^2C-based bus.
21. The margin testing system of claim 20, wherein said I^2C bus is an Intelligent Platform Management Bus (IPMB).	75. The margin testing system of claim 74, wherein said I^2C bus is an IPMB.
22. A electronic system, comprising a margin testing system for margin testing one or more components of the electronic system, said margin testing system comprising: a fault bypass module incorporated in said electronic system, said fault bypass module configured to intercept and mask signals indicative of one or more faults associated with one or more of said components during margin testing of said electronic system, stem; and an internal controller in communication with said fault bypass module, said internal controller configured to transmit a command to said fault bypass module to initiate masking of said	55. In an electronic system, a system for margin testing one or more components of the computer system, comprising: a fault bypass module incorporated in said electronic system, said fault bypass module masking signals indicative of faults associated with one or more of said components during margin testing of said electronic system. 58. The margin testing system of claim 55, further comprising: a controller internal to said electronic system and in communication with said fault bypass module, said controller transmitting a command to said fault bypass module for initiating

fault signals by said module.	masking of said fault signals by said module.
23. The electronic system of claim 22, wherein said controller is a Baseboard Management Controller (BMC).	72. The margin testing system of claim 58, wherein said controller comprises: a BMC
24. A method of masking faults during margin testing of an electronic system, comprising: intercepting one or more signals each indicative of one or more faults associated with one or more components of said electronic system during margin testing, thereof; and generating signals indicative of absence of said faults thereby masking said intercepted signals. 25. The method of claim 24, further comprising: transmitting at least one of said one or more fault signals to a power control element in absence of margin testing.	55. In an electronic system, a system for margin testing one or more components of the computer system, comprising: a fault bypass module incorporated in said electronic system, said fault bypass module masking signals indicative of faults associated with one or more of said components during margin testing of said electronic system. 63. The margin testing system of claim 55, further comprising: a power control element in communication with said fault bypass module, said fault bypass module transmitting one of more of said fault signals to said power control element in absence of margin testing and masking said one or more fault signals during margin testing of said electronic system.
26. The method of claim 25, wherein masking said intercepted signals, comprises: supplying to said power control element a signal indicative of absence of a fault indicated by said fault signals.	64. The margin testing system of claim 63, wherein said fault bypass module masks said fault signal by intercepting said fault signal and supplying to said power control element a signal indicative of absence of a fault indicated by said fault signal.
27. The method of claim 24, further comprising: generating an interrupt signal in response to a voltage associated with a power rail varying from a nominal value by more than a selected threshold.	65. The margin testing system of claim 61, wherein said at least one component is a power rail, and said hardware monitor generates an interrupt signal in response to a voltage associated with said power rail varying from a nominal value by more than a selected threshold.
28. The margin testing system of claim 27, further comprising: reducing power applied to said power rail in response to said interrupt signal in the absence of margin testing.	66. The margin testing system of claim 65, wherein said power control module lowers power applied to said voltage rail in response to said interrupt signal in the absence of margin testing.
29. The method claim 24, wherein intercepting one or more signals, comprises: intercepting a selected output signal of said one or more components; and wherein generating signals indicative of absence of said faults, comprises: generating a simulated signal corresponding to said intercepted output signal for transmittal to a hardware monitor.	69. The margin testing system of claim 61, wherein said fault bypass module intercepts a selected output signal of said at least one component and generates a simulated signal corresponding to said intercepted output signal for transmittal to said hardware monitor during margin testing of said component.
30. The method of claim 24, wherein said electronic system is a computer server.	70. The margin testing system of claim 55, wherein said electronic system comprises a computer system. 71. The margin testing system of claim 69, wherein said computer system is a computer server.
31. A system comprising: means for intercepting at least one signal indicative of at least one fault associated with at least one component of an electronic system during margin testing thereof; and means for masking said intercepted at least one signal by generating at least one signal indicative of absence of said at least one fault.	55. In an electronic system, a system for margin testing one or more components of the computer system, comprising: a fault bypass module incorporated in said electronic system, said fault bypass module masking signals indicative of faults associated with one or more of said components during margin testing of said electronic system. 63. The margin testing system of claim 55, further comprising: a power control element in communication with said fault bypass module, said fault bypass module transmitting one of more of said fault signals to said power control element in absence of margin testing and masking said one or more fault signals during margin testing of said electronic system. 64. The margin testing system of claim 63, wherein said fault bypass module masks said fault signal by intercepting said fault signal and supplying to said power control element a signal indicative of absence of a fault indicated by said fault signal.

32. A computer server, comprising a margin testing system for margin testing one or more components of the computer server, the margin testing system comprising: a fault bypass module incorporated in said computer server, said fault bypass module configured to mask signals indicative of one or more faults associated with one or more of said components during margin testing of said computer server.	55. In an electronic system, a system for margin testing one or more components of the computer system, comprising: a fault bypass module incorporated in said electronic system, said fault bypass module masking signals indicative of faults associated with one or more of said components during margin testing of said electronic system. 70. The margin testing system of claim 55, wherein said electronic system comprises a computer system. 71. The margin testing system of claim 69, wherein said computer system is a computer server.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-5, 6-8, 13, 16, 22, 24-27, 29-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushige (US 2003/0101020 A1) in view of NEC CORP (JP 2000172536A).

Regarding claims 1, 24, 31, and 32, Matsushige discloses a system for margin testing one or more components of an electronic system (Abstract), comprising a fault bypass module (port bypass circuit) incorporated in said electronic system, said fault bypass module configured to indicate of one or more faults associated with one or more of said components during margin testing of said electronic system ([0143]-[0145]).

Regarding claim 2, Matsushige discloses at least one of said one or more faults corresponds to an operating parameter associated with at least one of said one or more components crossing a selected threshold ([0057]-[0061], [0128]).

Regarding claim 3, Matsushige discloses said operating parameter is any of voltage ([0066]).

Regarding claim 4, Matsushige discloses a controller (15) incorporated in said electronic system and in communication with said fault bypass module, said controller configured to transmit a command to said fault bypass module to initiate masking of said fault signals by said module ([0055]-[0057], [0062]).

Regarding claim 6, Matsushige discloses said fault bypass module permits normal processing of said fault signals during normal operation of said electronic system ([0100]).

Regarding claim 7, Matsushige discloses a hardware monitor (micro processor 15) configured to communication with said controller and with at least one of said one or more components, and to generate a fault signal in response to an occurrence of a fault associated with said at least one component ([0088]-[0091]).

Regarding claim 8, Matsushige discloses said hardware monitor is further configured to transmit said fault signal to said fault bypass module, and wherein said fault bypass module is further configured to mask said received fault signal during margin testing of said electronic device ([0088]).

Regarding claim 13, Matsushige discloses a programmable logic device programmed to provide masking of said fault signals (0141]).

Regarding claim 16, Matsushige discloses said electronic system comprises a computer system ([0066]).

Regarding claim 22, Matsushige discloses a system for margin testing one or more components of the electronic system (Abstract), comprising: a fault bypass module (port bypass circuit) incorporated in said electronic system, said fault bypass module configured to indicate of one or more faults associated with one or more of said components during margin testing of said electronic system ([0143]-[0145]), and an internal controller (15) in communication with said fault bypass module, said internal controller configured to transmi a command to said fault bypass module to initiate masking of said fault signals by said module ([0055]-[0057], [0062]).

Regarding claims 25-27, Matsushige discloses a power control element in absence of margin testing, supplying to said power control element a signal indicative of absence of a fault indicated by said fault signals, a voltage associated with a power rail varying from a nominal value by more than a selected threshold (e.g. [0055]-[0068], [0100]-[0113]).

Regarding claim 30, Matsushige discloses said electronic system is a computer server ([0066]).

Matsushige fails to teach a fault bypass module configured to intercept and mask signals indicative of one or more faults.

NEC teaches a mask controller (42) configured to intercept and mask signals indicative (masking of interrupt signal) of one or more faults (e.g. Abstract, [0008]-[0012]).

Regarding claim 5, NEC teaches said fault signals comprise: one or more interrupt signals (e.g. Abstract, [0008]-[0012]).

Regarding claim 29, NEC teaches intercepting one or more signals, comprises: intercepting a selected output signal of said one or more components; and wherein generating signals indicative of absence of said faults, comprises: generating a simulated signal corresponding to said intercepted output signal for transmittal to a hardware monitor (e.g. [0014]-[0021]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a mask controller (42) configured to intercept and mask signals as taught by NEC in a margin test method of Matsushige for the purpose of providing a mask controller (42) controls the masking of interrupt signal, based on failure generation indication output by CPU (NEC, Abstract).

7. Claim 18-21 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushige (US 2003/0101020 A1) in view of NEC CORP (JP 2000172536A) as applied to claim 1 above, and further in view of Hawkins et al. (US 2003/0130969 A1).

Regarding claims 18-21 and 23, Matsushige fails to disclose a controller comprises a Baseboard Management Controller (BMC), wherein said communication bus is an Inter-Integrated Circuit bus (I^2C bus), wherein said I^2C bus is Intelligent Platform Management Bus (IPMB).

Hawkins et al. disclose a controller comprises a Baseboard Management Controller (BMC) ([0015]-[0017]), wherein said communication bus is an Inter-Integrated Circuit bus (I^2C bus)([0006]), wherein said I^2C bus is IPMB ([0013]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a Baseboard Management Controller (BMC), an Inter-Integrated Circuit bus (I^2C bus), wherein said I^2C bus is Intelligent Platform Management Bus (IPMB) as taught by Hawkins et al. in a margin test method of Matsushige in view of NEC for the purpose of providing a star Intelligent Platform Management Bus Topology.

Response to Arguments

8. Applicant's arguments filed 02/15/2005 have been fully considered but they are not persuasive.

-Applicant argues that the prior did not teach "intercept and mask signals indicative of faults" as citied in claims 1 and 24.

Examiner position is that NEC teaches a mask controller (42) configured to intercept and mask signals indicative (masking of interrupt signal) of one or more faults (e.g. Abstract, [0008]-[0012]).

-Applicant argues that the prior did not teach "a fault bypass module incorporated in said electronic system, said fault bypass module configured to intercept and mask signals indicative of one or more faults associated with one or more of said components during margin testing of said electronic system" as citied in claim 22.

Examiner position is that Matsushige and NEC in combination as discussed above, teaches a fault bypass module incorporated in said electronic system, said fault bypass module configured to intercept and mask signals indicative of one or more faults

associated with one or more of said components during margin testing of said electronic system.

Conclusion

9. Specifically NEC CORP (JP 2000172536A) and Robertson et al. have been added to second ground of rejection.

Contact Information

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John H Le whose telephone number is 571-272-2275. The examiner can normally be reached on 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E Barlow can be reached on 571-272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John H. Le
Patent Examiner-Group 2863
May 12, 2005

MICHAEL NGHIEM
PRIMARY EXAMINER